CLAIMS

What is claimed is:

1. An apparatus for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the apparatus comprising:

a computer configured to execute a rules checker program, the rules checker program receiving input relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the rules checker program analyzing the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

2. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the rules checker program processing the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths, the rules checker program utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer, the rules checker program determining noise levels on the inputs, the rules checker program comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

3. The apparatus of claim 2, wherein the rules checker program generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first representation of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the rules checker program determines noise levels on the first and second inputs and compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

4. The apparatus of claim 3, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access a third and fourth threshold values stored in the memory device, wherein the

rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

5. The apparatus of claim 4, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access a fifth and sixth threshold values stored in the memory device, wherein when the first input is high, the rules checker program determines the noise level on the first input and compares the determined noise level to the fifth threshold value, wherein when the first input is low, the rules checker program determines the noise level on the first input and compares the determined noise level to the sixth threshold value, wherein the results of the comparisons are used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise

immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

6. The apparatus of claim 5, wherein the rules checker program processes the widths of the P and N field effect transistors by generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the rules checker program determines the noise level on the second input and compares the determined noise level to the seventh threshold value, wherein when the second input is high, the rules checker program determines the noise level on the second input and compares the determined noise level to the eighth threshold value, the rules checker program using the results of the comparisons to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

7. The apparatus of claim 1, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, wherein the rules checker program generates first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein the rules checker program utilizes the largest and the smallest of all of the ratios to obtain first, second, third and fourth threshold values, respectively, from a memory device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs to determine whether or not the gate meets acceptable noise immunity requirements.

8. A method for evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the method comprising the steps of:

receiving input in a computer relating to characteristics of a static gate contained in the integrated circuit, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors; and

analyzing the widths of the field effect transistors in the computer to determine whether or not the gate has an acceptable noise immunity, wherein the computer executes a rules checker program which analyzes the widths to determine whether or not the gate has an acceptable noise immunity.

9. The method of claim 8, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the analyzing step being performed by the rules checker program further comprising the steps of:

processing the widths of the P field effect transistor and of the N field effect transistor to obtain at least a first numerical value relating to the widths;

utilizing the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

determining noise levels on the input terminals; and

comparing the determined noise levels with the threshold values read out of the memory device and using the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

10. The method of claim 9, wherein the processing step includes the step of generating a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the rules checker program to access the first and second threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are high and compares the determined noise levels to the first and second threshold values, respectively, to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first model, the rules checker program determines that the gate has an acceptable immunity to noise.

11. The method of claim 10, wherein the processing step further includes the step of generating a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the rules checker program to access third and fourth threshold values stored in the memory device, wherein the rules checker program determines noise levels on the first and second inputs when the first and second inputs are low and compares the determined noise levels to the third and fourth threshold values, respectively, to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the rules checker program determines that the gate has an acceptable noise immunity.

12. The method of claim 11, wherein the wherein the processing step further includes the step of generating a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the rules checker program to access fifth and sixth threshold values stored in

the memory device, wherein the rules checker program determines the noise level on the first input when the first input is high and compares the determined noise level to the fifth and sixth threshold values, and wherein the rules checker program determines the noise level on the second input when the second input is high and compares the determined noise level to the fifth and sixth threshold values, the results of the comparison operations being used by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the rules checker program determines that the gate has an acceptable noise immunity.

13. The method of claim 12, wherein the wherein the processing step further includes the step of generating a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the rules checker program obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the rules checker program to access seventh and eighth threshold values stored in the memory device, wherein the rules checker program determines the noise level on the second input when the second input is low and compares the determined noise levels to the seventh and eighth threshold values, and wherein the rules checker program determines the noise level on the first input when the first input is low and compares the determined noise levels to the seventh and eighth threshold

values, the rules checker program using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the rules checker program determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the rules checker program determines that the gate has an acceptable noise immunity.

14. The method of claim 9, wherein the processing step includes the step of generating first, second, third and fourth models of the gate in order to process the widths of the P and N field effect transistors, the first, second, third and fourth models of the gate each consisting of a single N field effect transistor and a single P field effect transistor, wherein during the processing step the rules checker program obtains first, second, third and fourth ratios, the first ratio corresponding to a ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value, the second ratio corresponding to a ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the third ratio corresponding to a ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the fourth ratio corresponding to a ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, wherein during the utilizing step the rules checker program utilizes the largest and the smallest of all of the ratios to obtain the first, second, third and fourth threshold values from the memory

device, the first and second threshold values corresponding to the largest of the ratios, the third and fourth threshold values corresponding to the smallest of the ratios, the threshold values being compared to noise levels on the inputs of the gate for particular logic states, the results of the comparison operations being utilized by the rules checker program to determine whether or not the gate meets acceptable noise immunity requirements.

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15. A rules checker computer program embodied on a computer-readable medium, the program evaluating a gate to determine whether or not the gate has an acceptable immunity to noise, the gate comprising at least two field effect transistors, each field effect transistor having a width, the characteristics including the widths of the field effect transistors, the program comprising:

code which analyzes the widths of the field effect transistors to determine whether or not the gate has an acceptable noise immunity.

16. The program of claim 15, wherein the gate comprises at least one N field effect transistor and at least one P field effect transistor, the gate comprising at least first and second input terminals for receiving respective first and second input signals, the code comprising:

a first code segment which processes the widths of the P field effect transistor and of the N field effect transistor to obtain a first numerical value relating to the widths;

a second code segment which utilizes the first numerical value to access first and second threshold values stored in a memory device in communication with the computer;

a third code segment which determines noise levels on the input terminals; and

a fourth code segment which compares the determined noise levels with the threshold values read out of the memory device and uses the results of the comparison to determine whether or not the gate has an acceptable immunity to noise.

17. The program of claim 16, wherein the first code segment includes model generating code which generates a first model of the gate in order to process the widths of the P and N field effect transistors, the first model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a first ratio of the width of the P field effect transistor of the first model to the width of the N field effect transistor of the first model, the first ratio corresponding to the first numerical value used by the second code segment to access the first and second threshold values stored in the memory device, wherein when the first and second inputs are high, the third code segment determines noise levels on the first and second inputs and wherein the fourth code segment compares the determined noise levels to the first and second threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the first model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first model, the program determines that the gate has an acceptable immunity to noise.

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18. The method of claim 17, wherein the model generating code generates a second model of the gate, the second model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a second ratio of the width of the P field effect transistor of the second model to the width of the N field effect transistor of the second model, the second ratio corresponding to a second numerical value, the second numerical value being used by the second code segment to access a third and fourth threshold values stored in the memory device, wherein the third code segment determines noise levels on the first and second inputs when the first and second inputs are low and wherein the fourth code segment compares the determined noise levels to the third and fourth threshold values to determine whether or not the gate meets acceptable noise immunity requirements with respect to the second model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first and second models, the program determines that the gate has an acceptable noise immunity.

19. The program of claim 18, wherein the model generating code generates a third model of the gate, the third model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a third ratio of the width of the P field effect transistor of the third model to the width of the N field effect transistor of the third model, the third ratio corresponding to a third numerical value, the third numerical value being used by the second code segment to access fifth and sixth threshold values stored in the memory device, wherein when the

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first input is high, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the fifth threshold value, and wherein when the first input is low, the third code segment determines the noise level on the first input and wherein the fourth code segment compares the determined noise level to the sixth threshold value, the fourth code segment using the results of the comparison operations to determine whether or not the gate meets acceptable noise immunity requirements with respect to the third model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second and third models, the program determines that the gate has an acceptable noise immunity.

20. The program of claim 19, wherein the model generating code generates a fourth model of the gate, the fourth model of the gate consisting of a single N field effect transistor and a single P field effect transistor, the model generating code obtaining a fourth ratio of the width of the P field effect transistor of the fourth model to the width of the N field effect transistor of the fourth model, the fourth ratio corresponding to a fourth numerical value, the fourth numerical value being used by the second code segment to access seventh and eighth threshold values stored in the memory device, wherein when the second input is low, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level to the seventh threshold value, and wherein when the second input is high, the third code segment determines the noise level on the second input and wherein the fourth code segment compares the measured noise level

to the eighth threshold value, the fourth code segment using the results of the comparison to determine whether or not the gate meets acceptable noise immunity requirements with respect to the fourth model, wherein if the fourth code segment determines that the gate meets acceptable noise immunity requirements with respect to the first, second, third and fourth models, the program determines that the gate has an acceptable noise immunity.